FIG. 1A

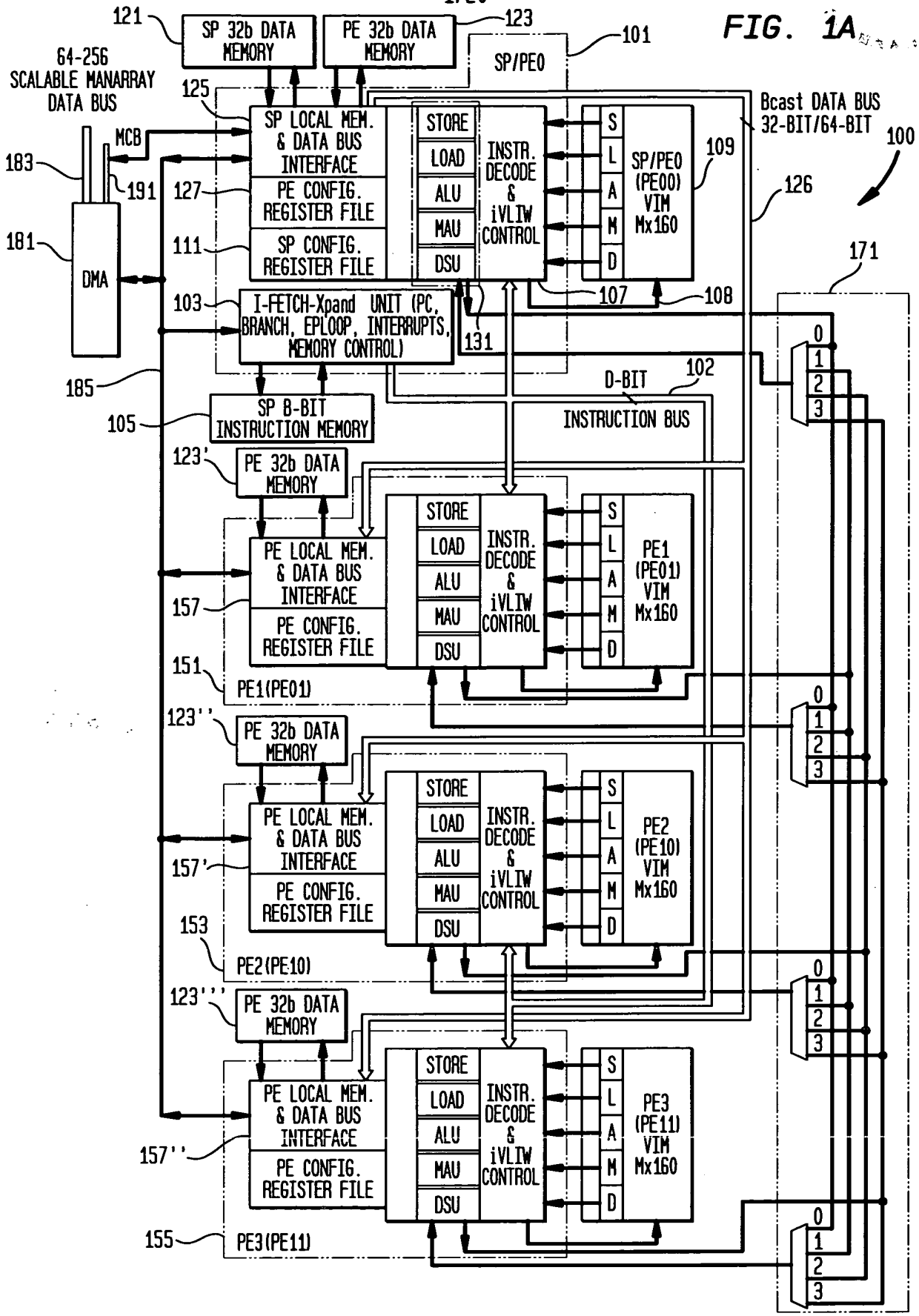

121
SP 32b DATA MEMORY
PE 32b DATA MEMORY
123
101
SP/PE0
64-256 SCALABLE MANARRAY DATA BUS
125
SP LOCAL MEM. & DATA BUS INTERFACE
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIM Mx160
109
Bcast DATA BUS 32-BIT/64-BIT
100
MCB
183
191
127
PE CONFIG. REGISTER FILE
126
181
DMA
111
SP CONFIG. REGISTER FILE
171
103
I-FETCH-Xpand UNIT (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL)
107
108
131
185
D-BIT
102
105
SP 8-BIT INSTRUCTION MEMORY
INSTRUCTION BUS
123'
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE
PE1 (PE01) VIM Mx160
157
151
PE1(PE01)
123''
PE2 (PE10) VIM Mx160
157'
153
PE2(PE10)
123'''
PE3 (PE11) VIM Mx160
157''
155
PE3(PE11)
0
1
2
3

FIG. 1B

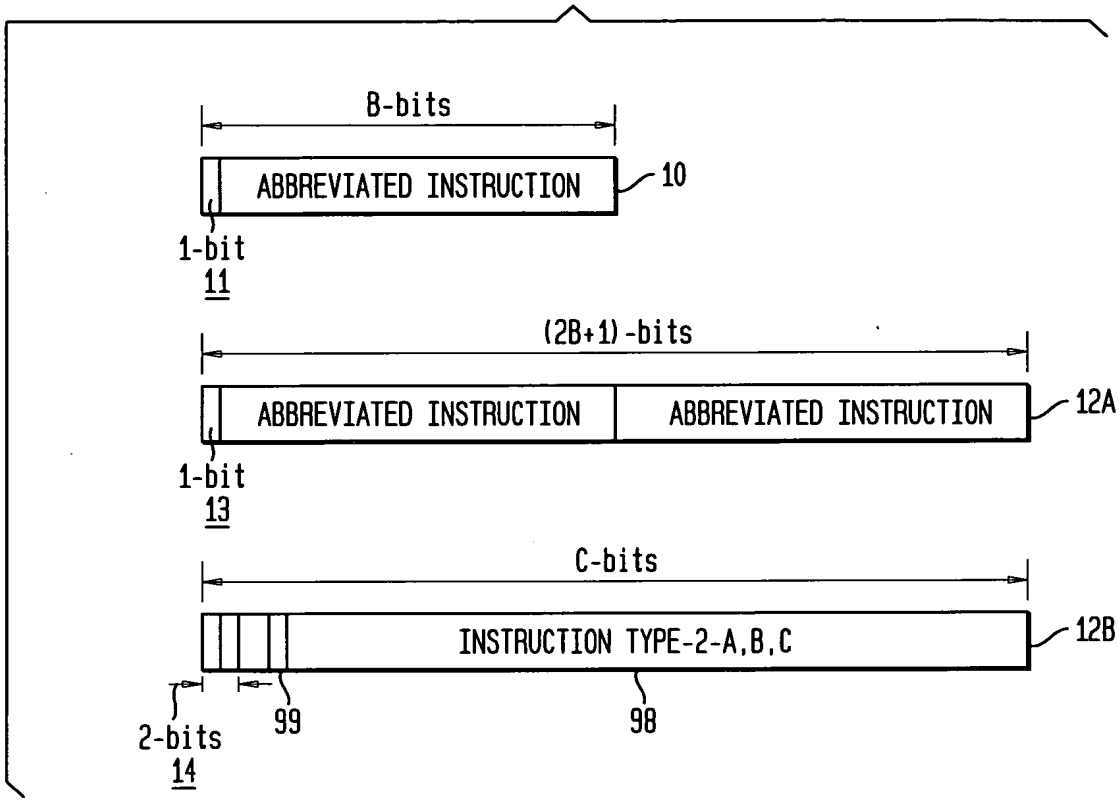

B-bits
ABBREVIATED INSTRUCTION
10
1-bit
11
(2B+1)-bits
ABBREVIATED INSTRUCTION
ABBREVIATED INSTRUCTION
12A
1-bit
13
C-bits
INSTRUCTION TYPE-2-A,B,C
12B
2-bits
14
99
98

FIG. 2

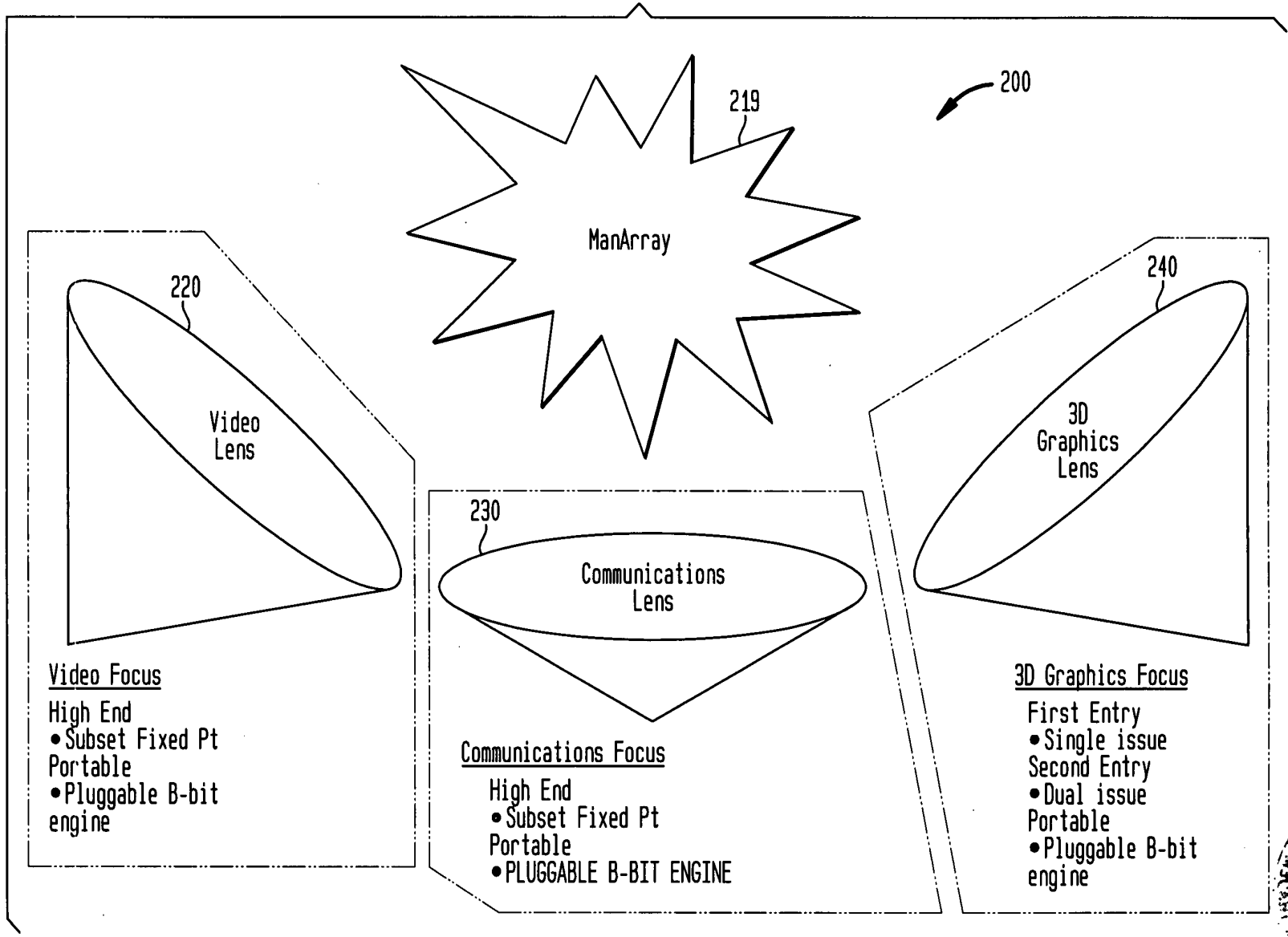

200
219
ManArray
220
Video Lens
240
3D Graphics Lens
230
Communications Lens
Video Focus
High End
• Subset Fixed Pt
Portable
• Pluggable B-bit engine
Communications Focus
High End
• Subset Fixed Pt
Portable
• PLUGGABLE B-BIT ENGINE
3D Graphics Focus
First Entry
• Single issue
Second Entry
• Dual issue
Portable
• Pluggable B-bit engine

FIG. 3A

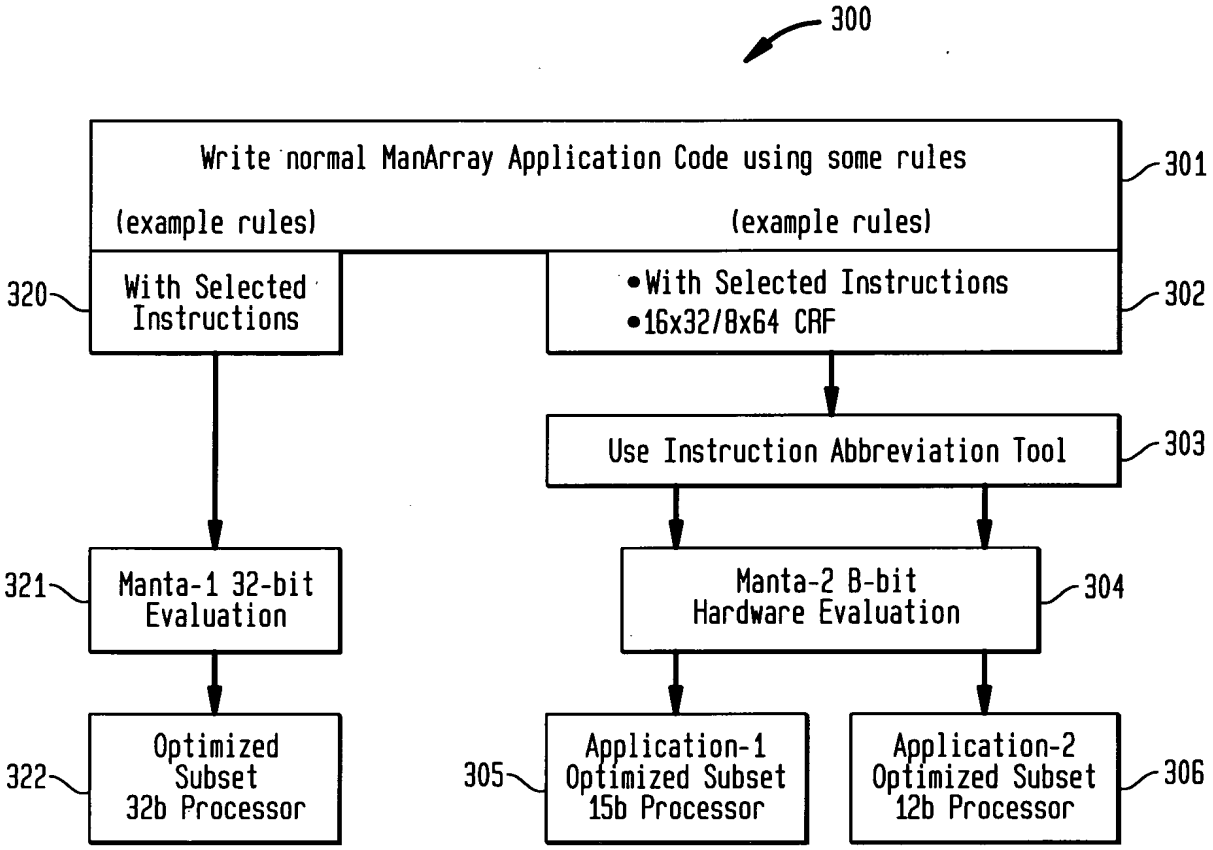

300
Write normal ManArray Application Code using some rules
301
(example rules)
(example rules)
320
With Selected Instructions
•With Selected Instructions
•16x32/8x64 CRF
302
Use Instruction Abbreviation Tool
303
321
Manta-1 32-bit Evaluation
Manta-2 8-bit Hardware Evaluation
304
322
Optimized Subset 32b Processor
305
Application-1 Optimized Subset 15b Processor
Application-2 Optimized Subset 12b Processor
306

FIG. 3B

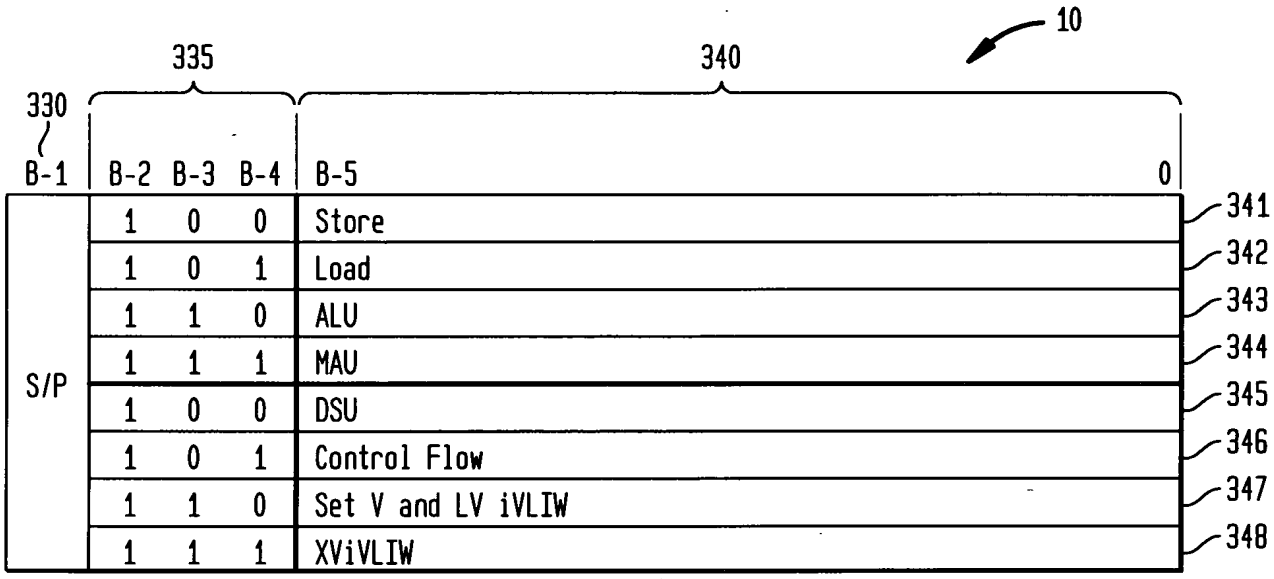

10
335
340
330
B-1
B-2 B-3 B-4
B-5
0
S/P
1 0 0 Store
1 0 1 Load
1 1 0 ALU
1 1 1 MAU
1 0 0 DSU
1 0 1 Control Flow
1 1 0 Set V and LV iVLIW
1 1 1 XViVLIW
341
342
343
344
345
346
347
348

FIG. 3C

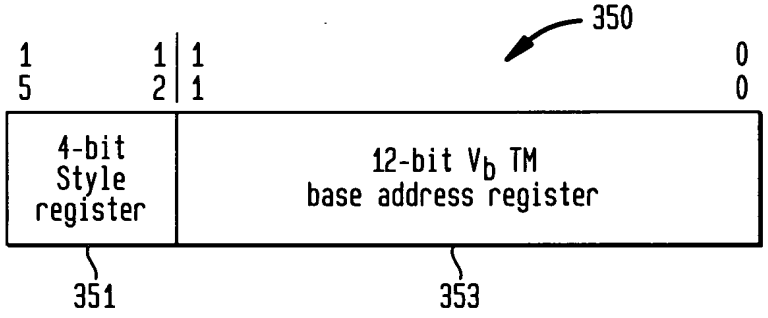

350
15
12
11
0
0
4-bit Style register
12-bit V_b TM base address register
351
353

FIG. 3D

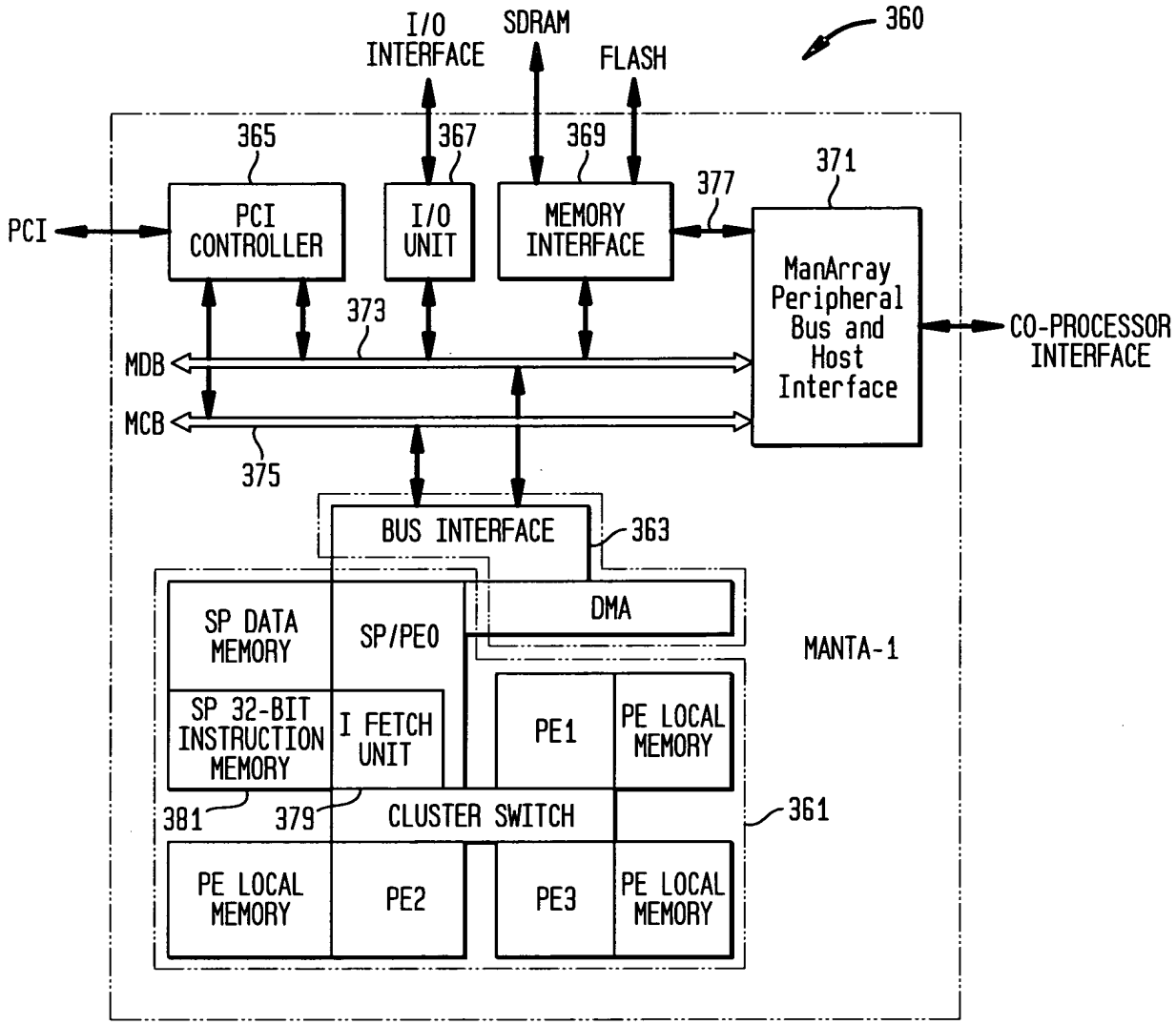
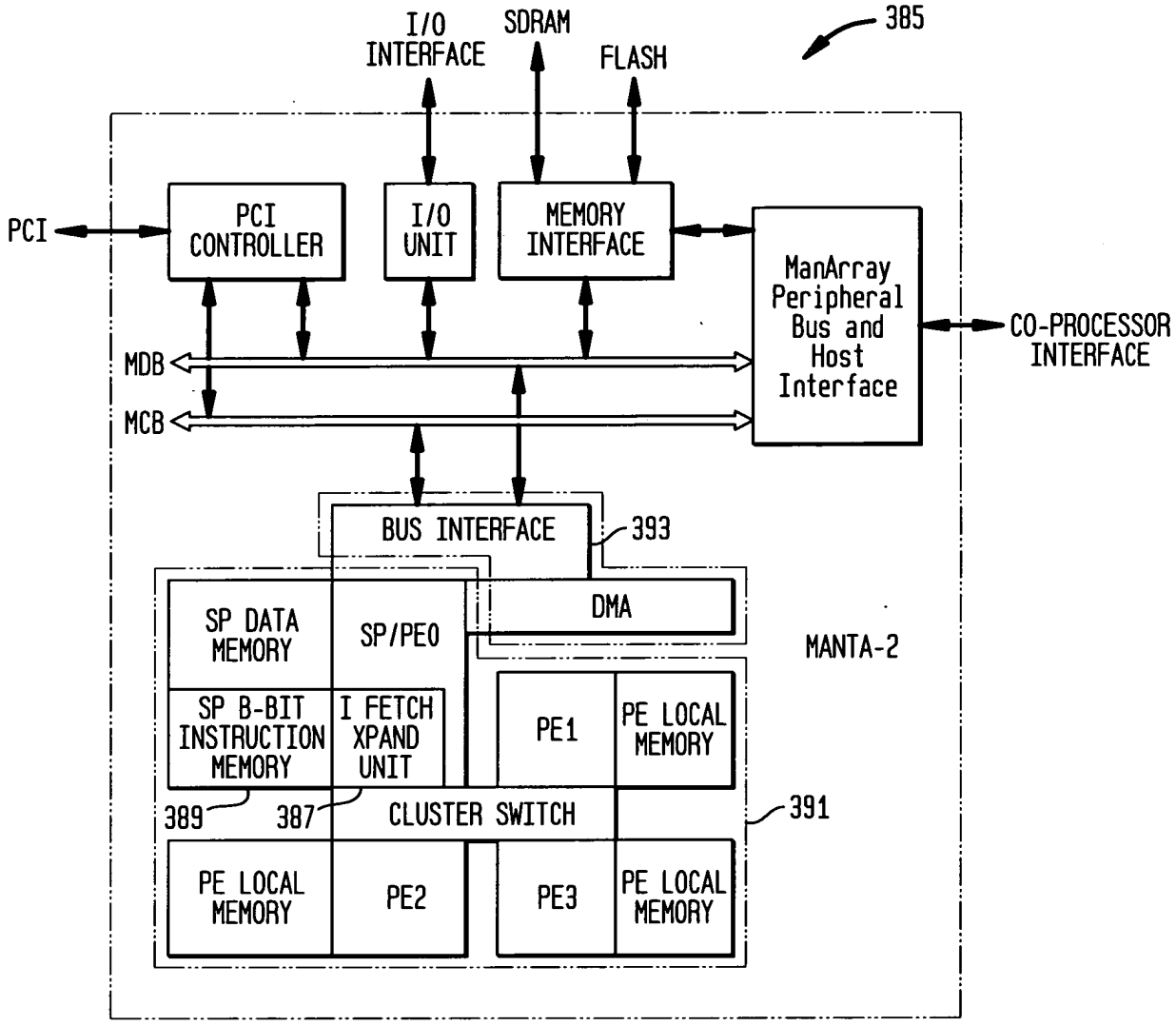

I/O INTERFACE
SDRAM
FLASH
360
365
367
369
371
377
PCI
PCI CONTROLLER
I/O UNIT
MEMORY INTERFACE
ManArray Peripheral Bus and Host Interface
CO-PROCESSOR INTERFACE
373
MDB
MCB
375
BUS INTERFACE
363
SP DATA MEMORY
SP/PE0
DMA
MANTA-1
SP 32-BIT INSTRUCTION MEMORY
I FETCH UNIT
PE1
PE LOCAL MEMORY
381
379
CLUSTER SWITCH
361
PE LOCAL MEMORY
PE2
PE3
PE LOCAL MEMORY

FIG. 3E


I/O INTERFACE
SDRAM
FLASH
385
PCI
PCI CONTROLLER
I/O UNIT
MEMORY INTERFACE
ManArray Peripheral Bus and Host Interface
CO-PROCESSOR INTERFACE
MDB
MCB
BUS INTERFACE
393
DMA
SP DATA MEMORY
SP/PE0
MANTA-2
SP B-BIT INSTRUCTION MEMORY
I FETCH XPAND UNIT
PE1
PE LOCAL MEMORY
389
387
CLUSTER SWITCH
391
PE LOCAL MEMORY
PE2
PE3
PE LOCAL MEMORY

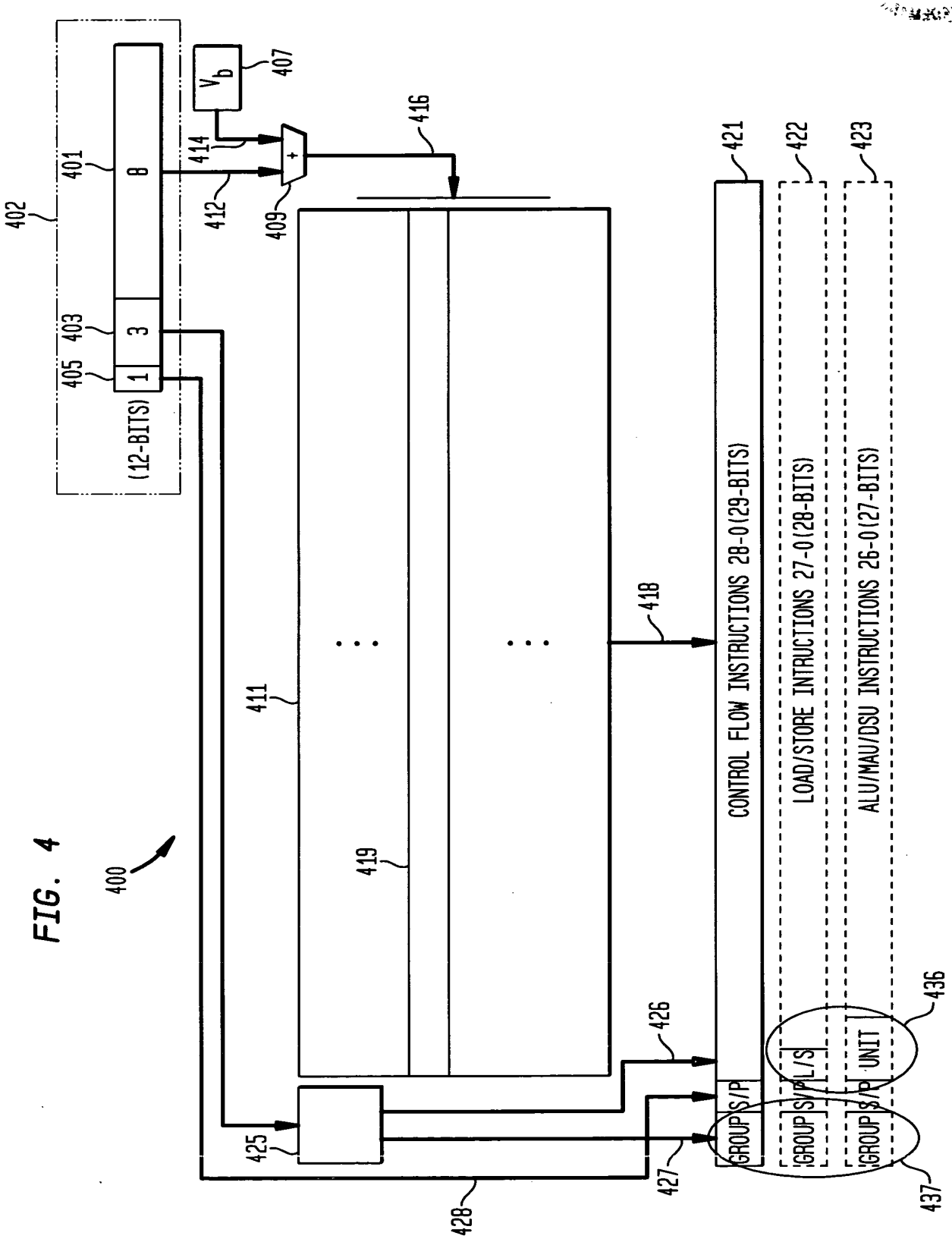

400
401
8
402
403
3
405
1
(12-BITS)
407
V_b
409
412
414
416
411
418
419
421
422
423
425
426
427
428
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS)
LOAD/STORE INTRUCTIONS 27-0(28-BITS)
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS)
GROUP
S/P
L/S
UNIT
436
437

FIG. 4

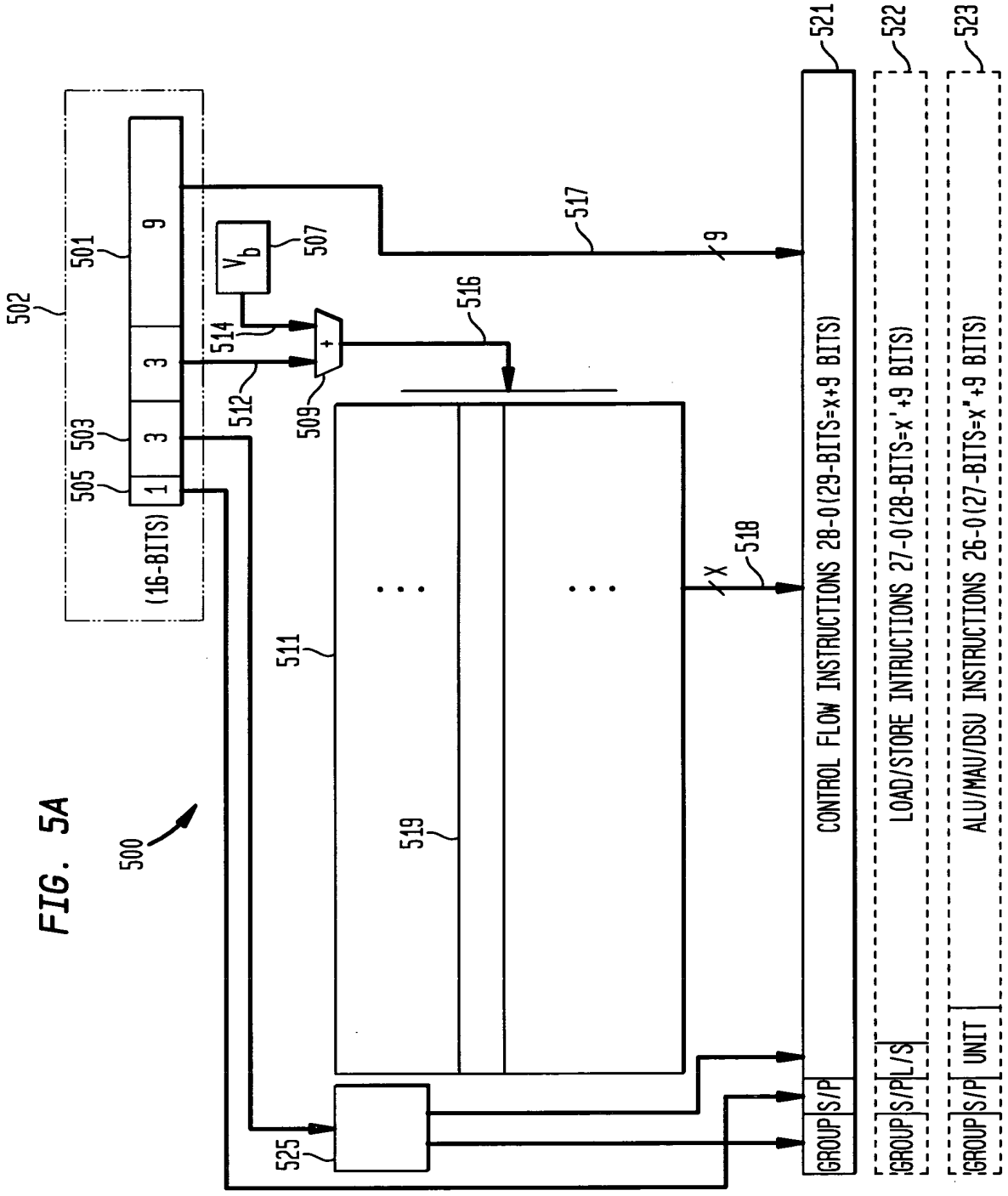

500
501
502
503
505
(16-BITS)
9
3
3
1
507
V_b
514
512
509
516
517
9
511
519
518
X
521
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+9 BITS)
GROUP S/P
522
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+9 BITS)
GROUP S/P L/S
523
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+9 BITS)
GROUP S/P UNIT
525

FIG. 5A

FIG. 5B

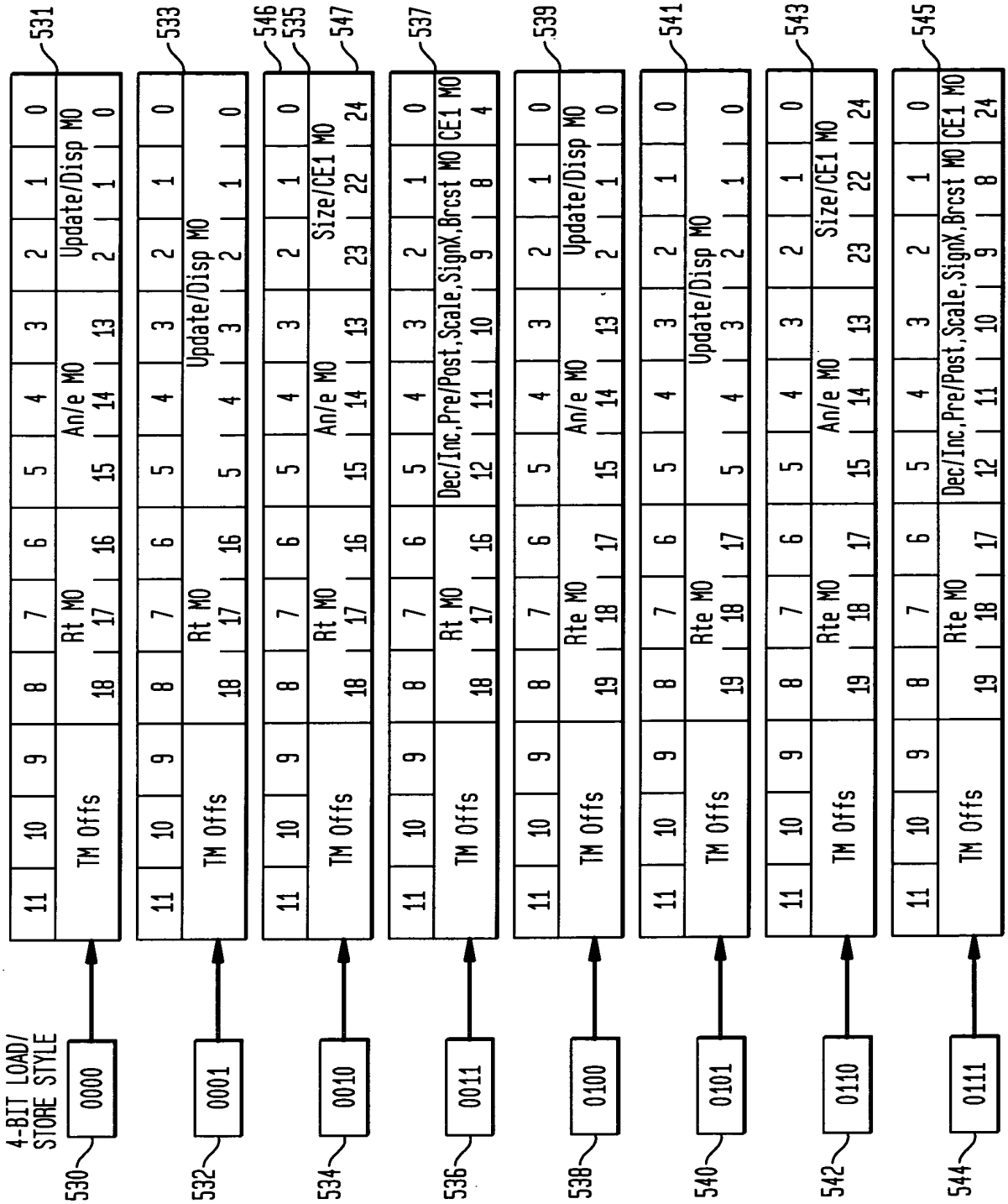

4-BIT LOAD/ STORE STYLE
0000
0001
0010
0011
0100
0101
0110
0111
TM Offs
Rt MO
An/e MO
Update/Disp MO
Rte MO
Size/CE1 MO
Dec/Inc,Pre/Post,Scale,SignX,Brcst MO
CE1 MO
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547

FIG. 5C

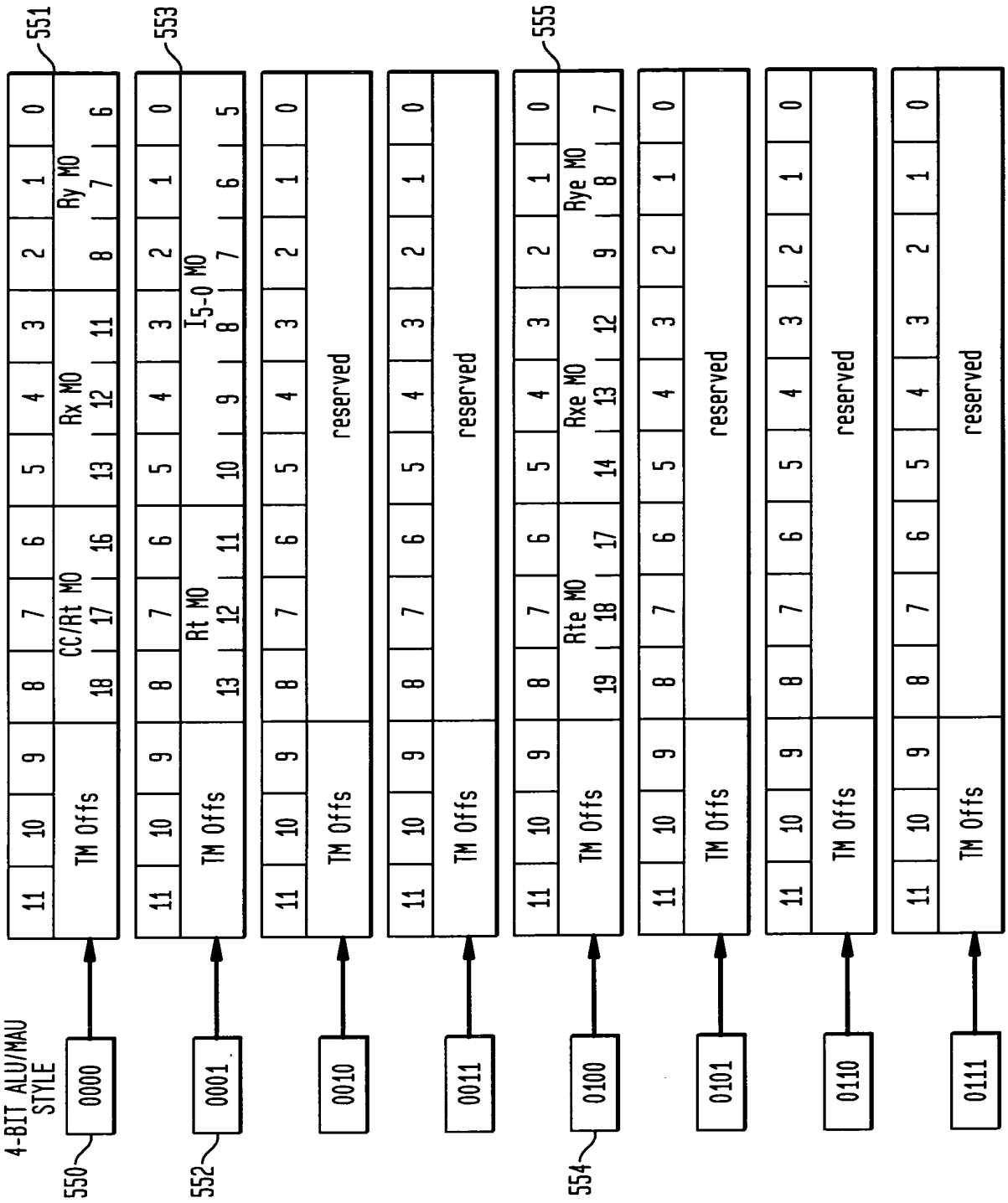
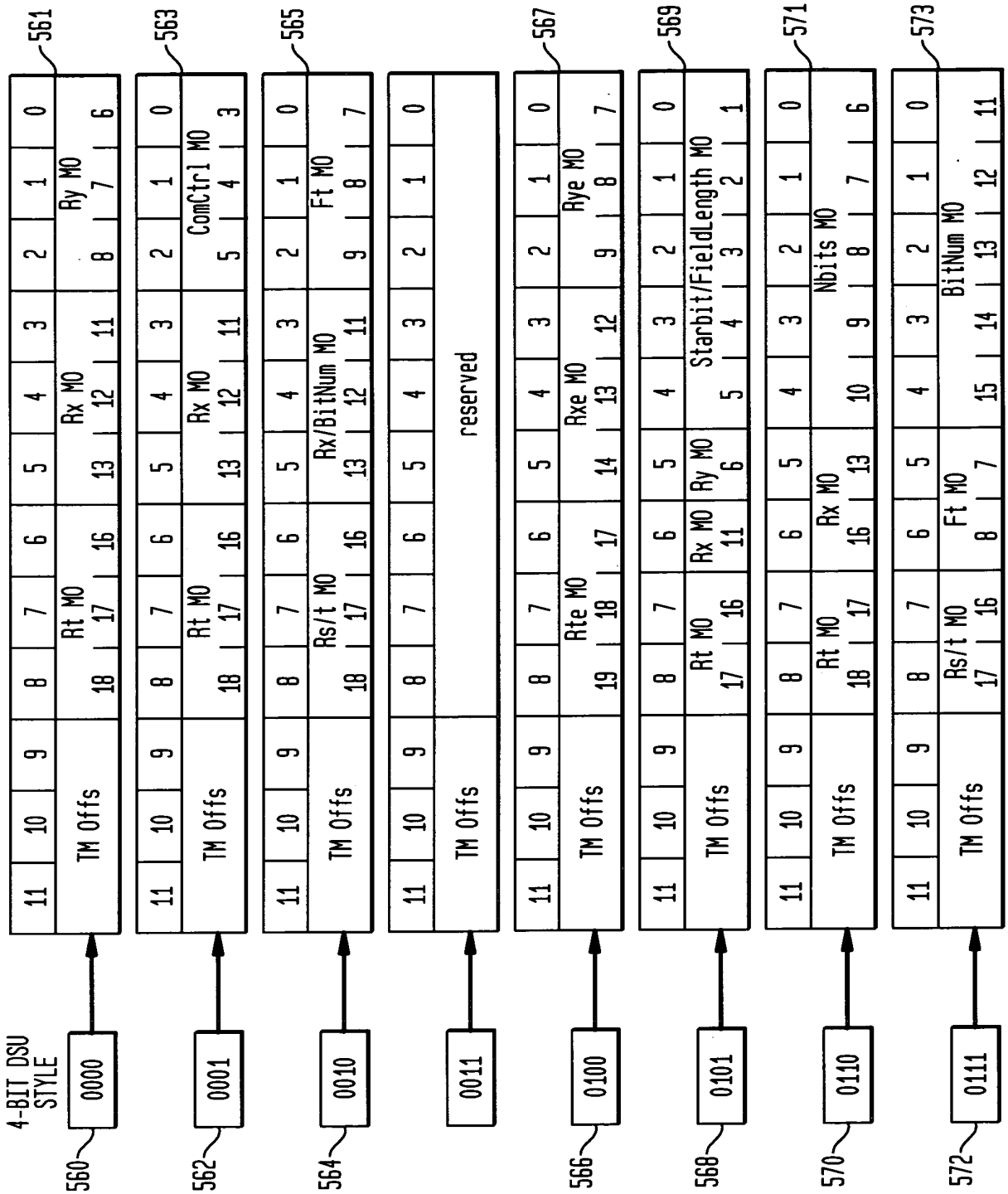

4-BIT ALU/MAU STYLE
0000
0001
0010
0011
0100
0101
0110
0111
550
552
554
551
553
555
TM Offs
CC/Rt MO
Rx MO
Ry MO
Rt MO
I5-0 MO
Rte MO
Rxe MO
Rye MO
reserved

FIG. 5D


4-BIT DSU STYLE
0000
0001
0010
0011
0100
0101
0110
0111
560
562
564
566
568
570
572
561
563
565
567
569
571
573
TM Offs
Rt MO
Rx MO
Rs/t MO
Rx/BitNum MO
reserved
Rte MO
Rxe MO
Starbit/FieldLength MO
Nbits MO
Ft MO
BitNum MO
Ry MO
ComCtrl MO
Rye MO

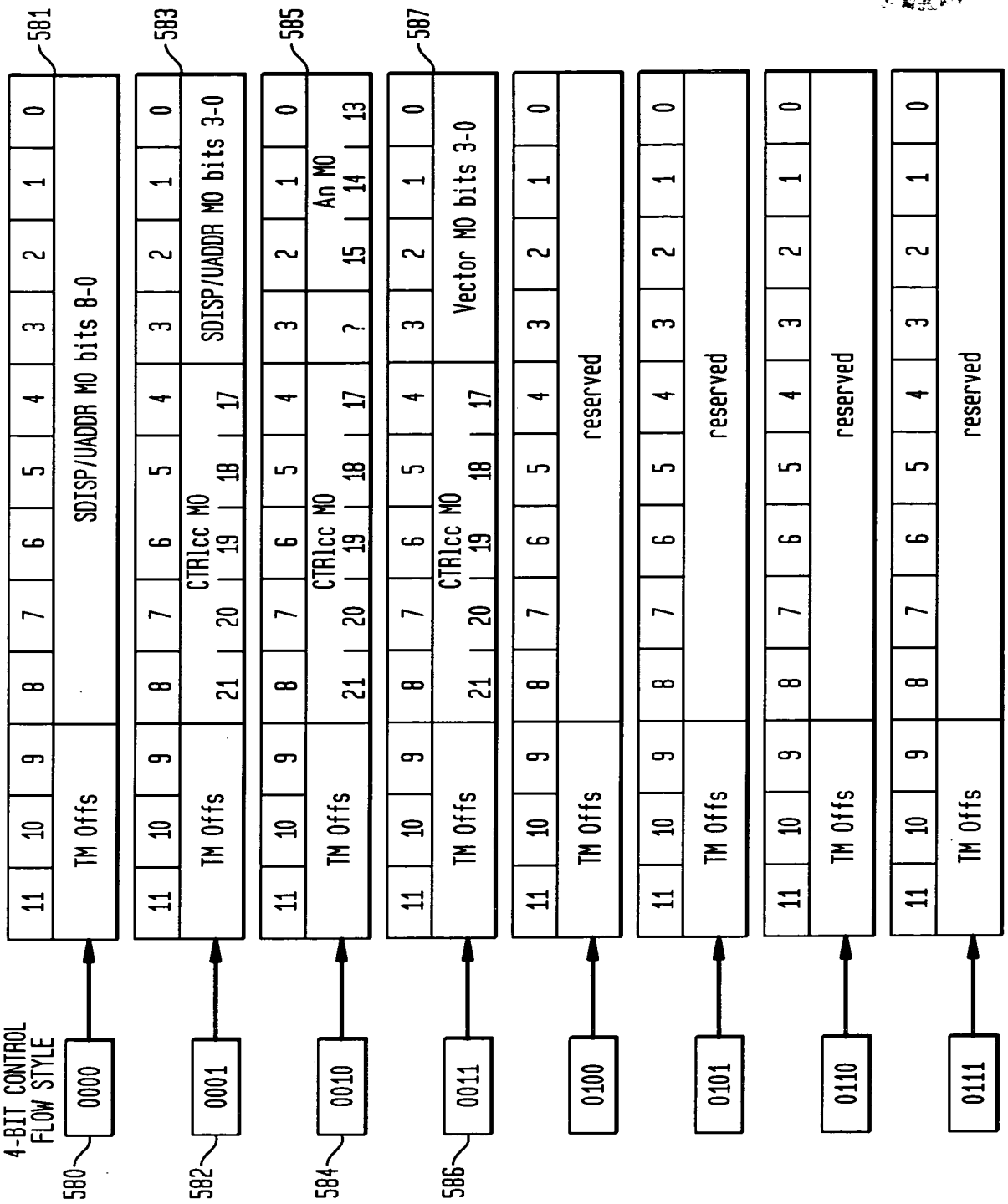

581
583
585
587
0 1 2 3 4 5 6 7 8 9 10 11
SDISP/UADDR MO bits 8-0
TM Offs
SDISP/UADDR MO bits 3-0
CTRlcc MO
17 18 19 20 21
An MO
13 14 15 ?
Vector MO bits 3-0
reserved
4-BIT CONTROL FLOW STYLE
0000
0001
0010
0011
0100
0101
0110
0111
580
582
584
586

FIG. 5E

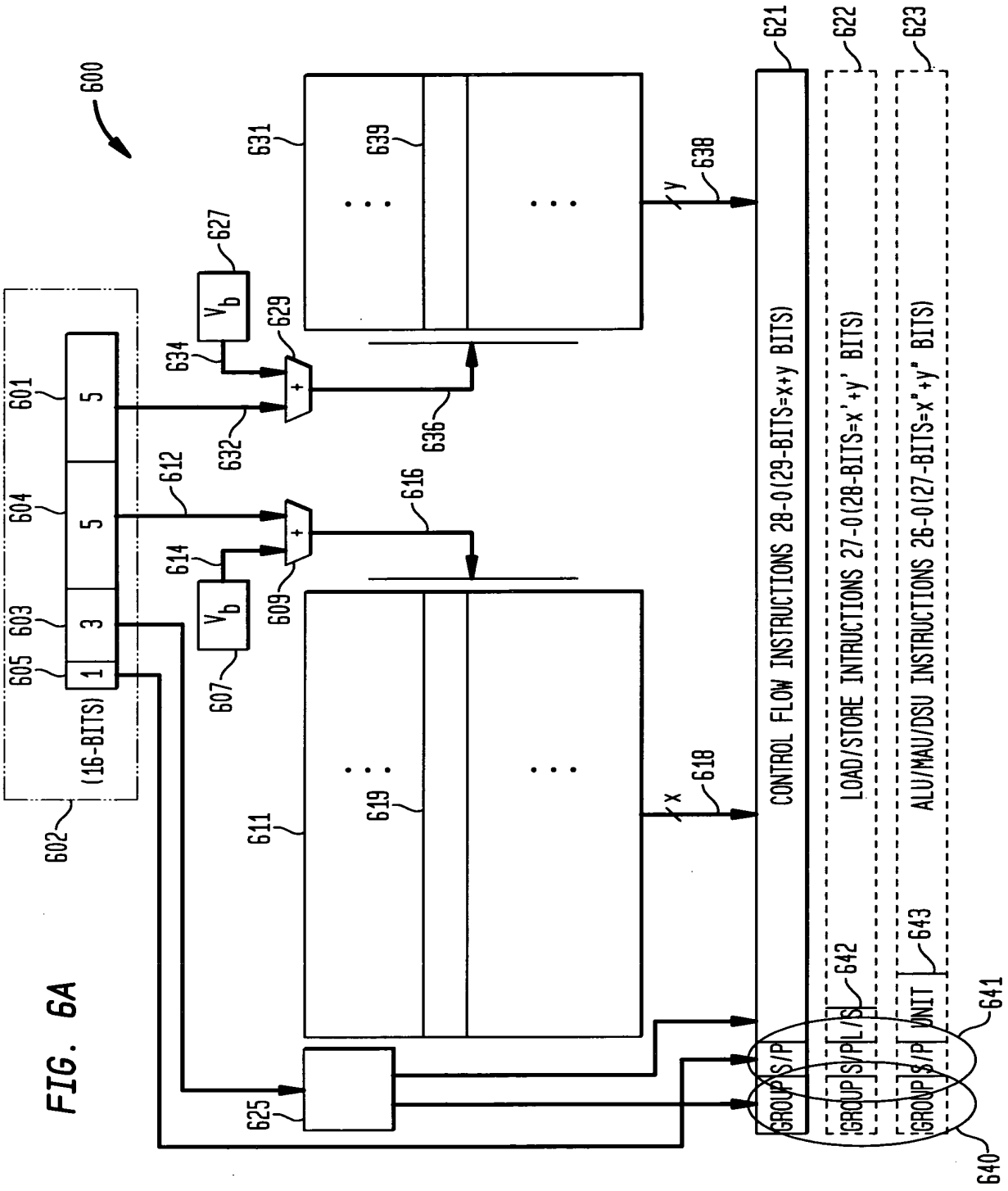
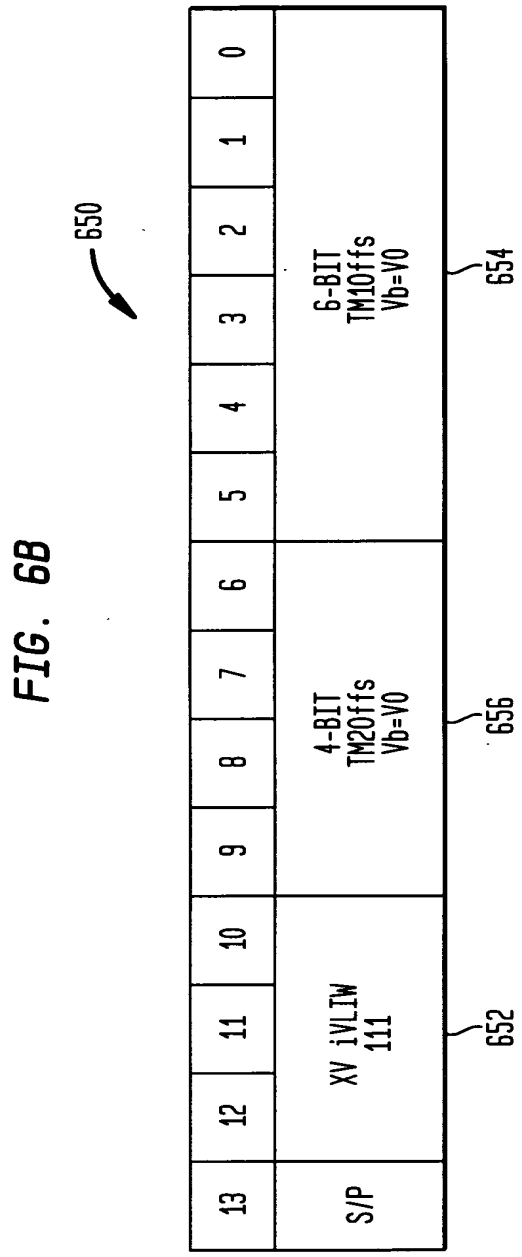

600
601
604
603
605
5
5
3
1
(16-BITS)
602
612
614
607
609
616
627
634
629
632
636
631
639
638
621
622
623
611
619
618
625
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+y BITS)
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+y' BITS)
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+y" BITS)
GROUP S/P
GROUP S/PL/S
GROUP S/P
UNIT
642
643
641
640

FIG. 6A

FIG. 6B


650
13
12
11
10
9
8
7
6
5
4
3
2
1
0
S/P
XV iVLIW
111
652
4-BIT
TM20ffs
Vb=V0
656
6-BIT
TM10ffs
Vb=V0
654

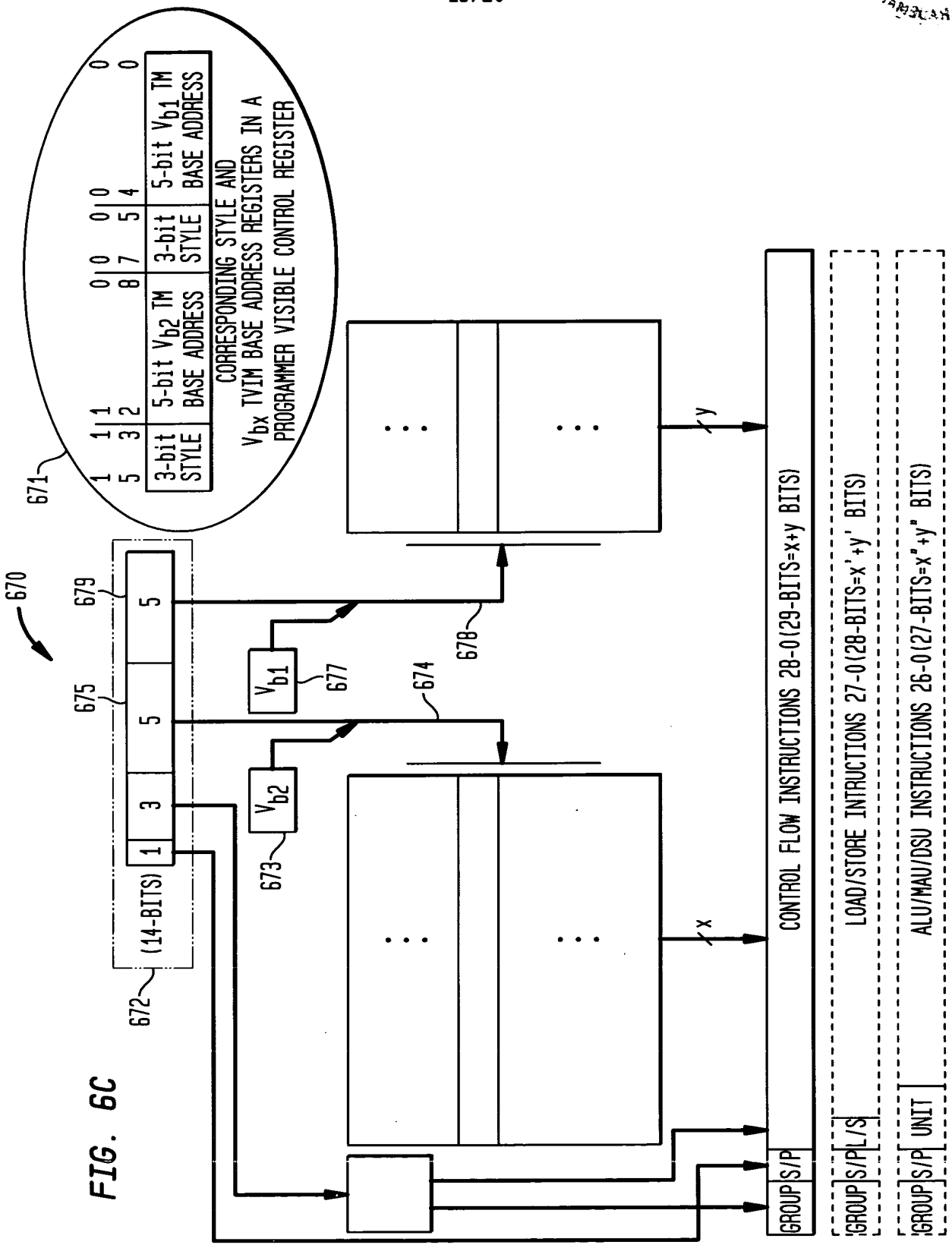

671
3-bit STYLE
5-bit V_{b2} TM BASE ADDRESS
3-bit STYLE
5-bit V_{b1} TM BASE ADDRESS
CORRESPONDING STYLE AND
V_{bx} TVIM BASE ADDRESS REGISTERS IN A
PROGRAMMER VISIBLE CONTROL REGISTER
670
679
675
672
(14-BITS)
673
V_{b2}
677
V_{b1}
674
678
x
y
GROUP S/P
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+y BITS)
GROUP S/P L/S
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+y' BITS)
GROUP S/P UNIT
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+y" BITS)

FIG. 6C

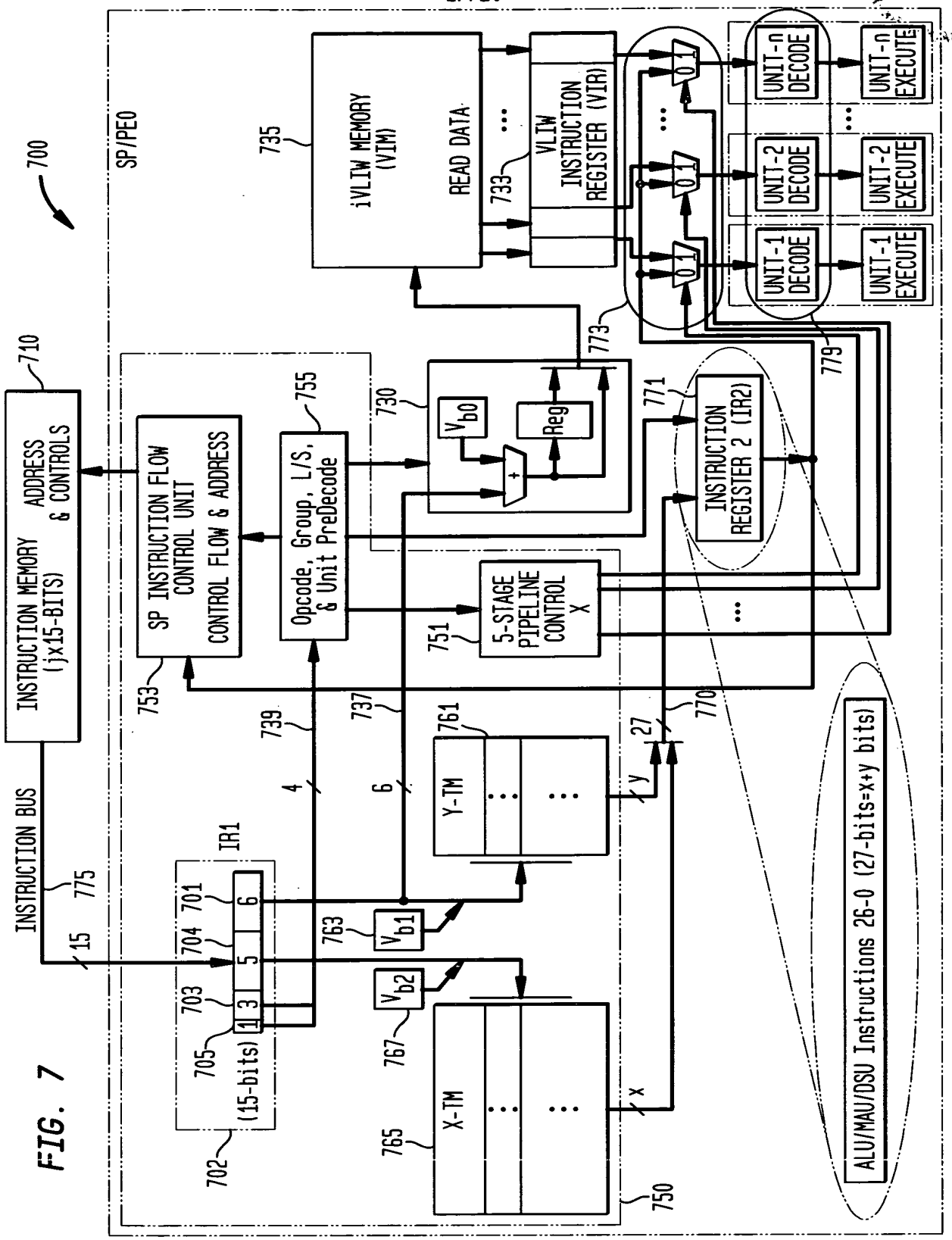

700
SP/PE0
735
iVLIW MEMORY (VIM)
READ DATA
733
VLIW INSTRUCTION REGISTER (VIR)
UNIT-n DECODE
UNIT-n EXECUTE
UNIT-2 DECODE
UNIT-2 EXECUTE
UNIT-1 DECODE
UNIT-1 EXECUTE
773
779
710
INSTRUCTION MEMORY (jx15-BITS)
ADDRESS & CONTROLS
SP INSTRUCTION FLOW CONTROL UNIT
CONTROL FLOW & ADDRESS
753
755
Opcode, Group, L/S, & Unit PreDecode
730
Vb0
Reg
771
INSTRUCTION REGISTER 2 (IR2)
751
5-STAGE PIPELINE CONTROL X
739
737
761
Y-TM
27
770
INSTRUCTION BUS
775
15
IR1
701
704
703
705
(15-bits)
702
763
Vb1
Vb2
767
765
X-TM
750
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

FIG. 7

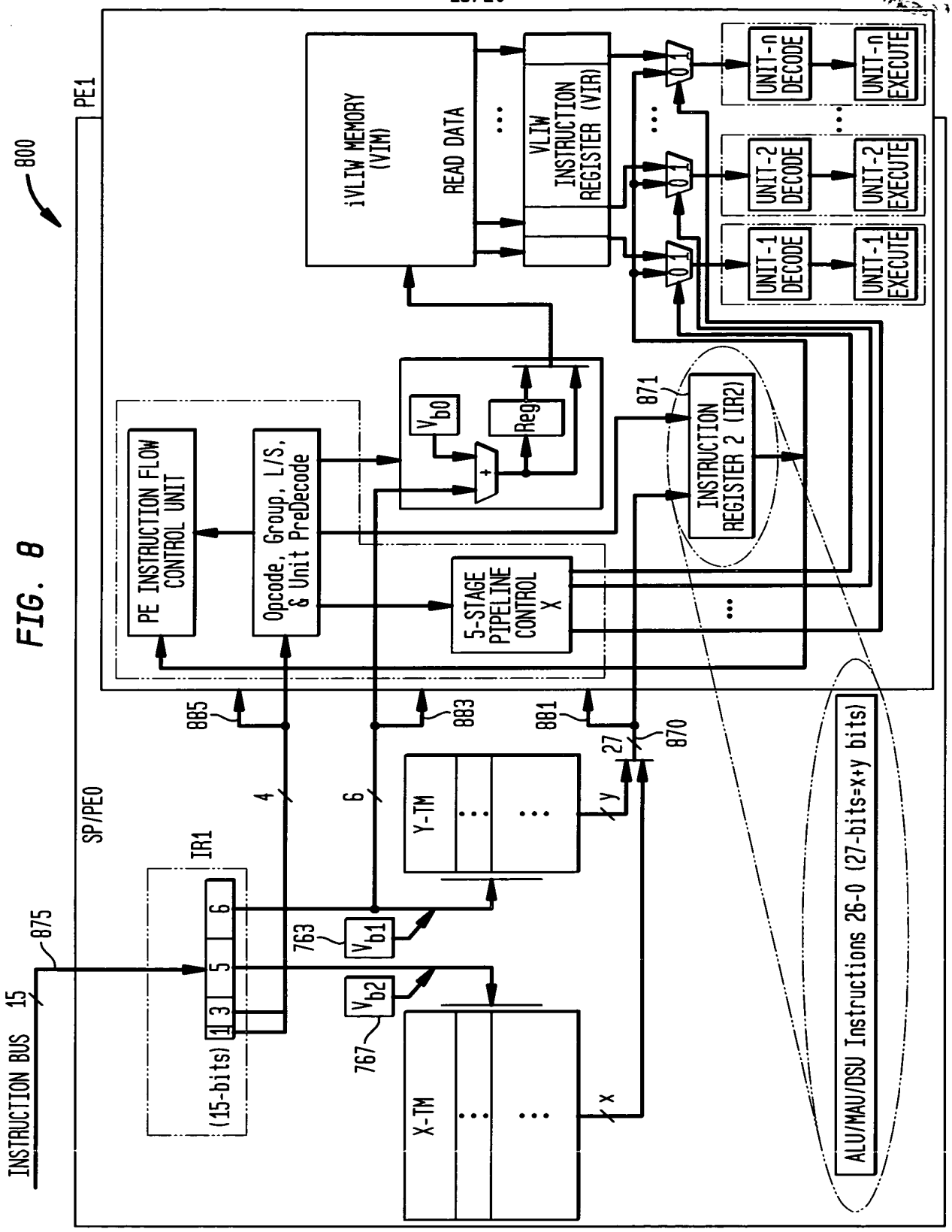

800
PE1
SP/PE0
iVLIW MEMORY (VIM)
READ DATA
VLIW INSTRUCTION REGISTER (VIR)
UNIT-n DECODE
UNIT-n EXECUTE
UNIT-2 DECODE
UNIT-2 EXECUTE
UNIT-1 DECODE
UNIT-1 EXECUTE
PE INSTRUCTION FLOW CONTROL UNIT
Opcode, Group, L/S, & Unit PreDecode
Vb0
Reg
INSTRUCTION REGISTER 2 (IR2)
871
5-STAGE PIPELINE CONTROL X
885
883
881
870
27
Y-TM
y
IR1
(15-bits)
INSTRUCTION BUS
15
875
763
Vb1
767
Vb2
X-TM
x
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

FIG. 8

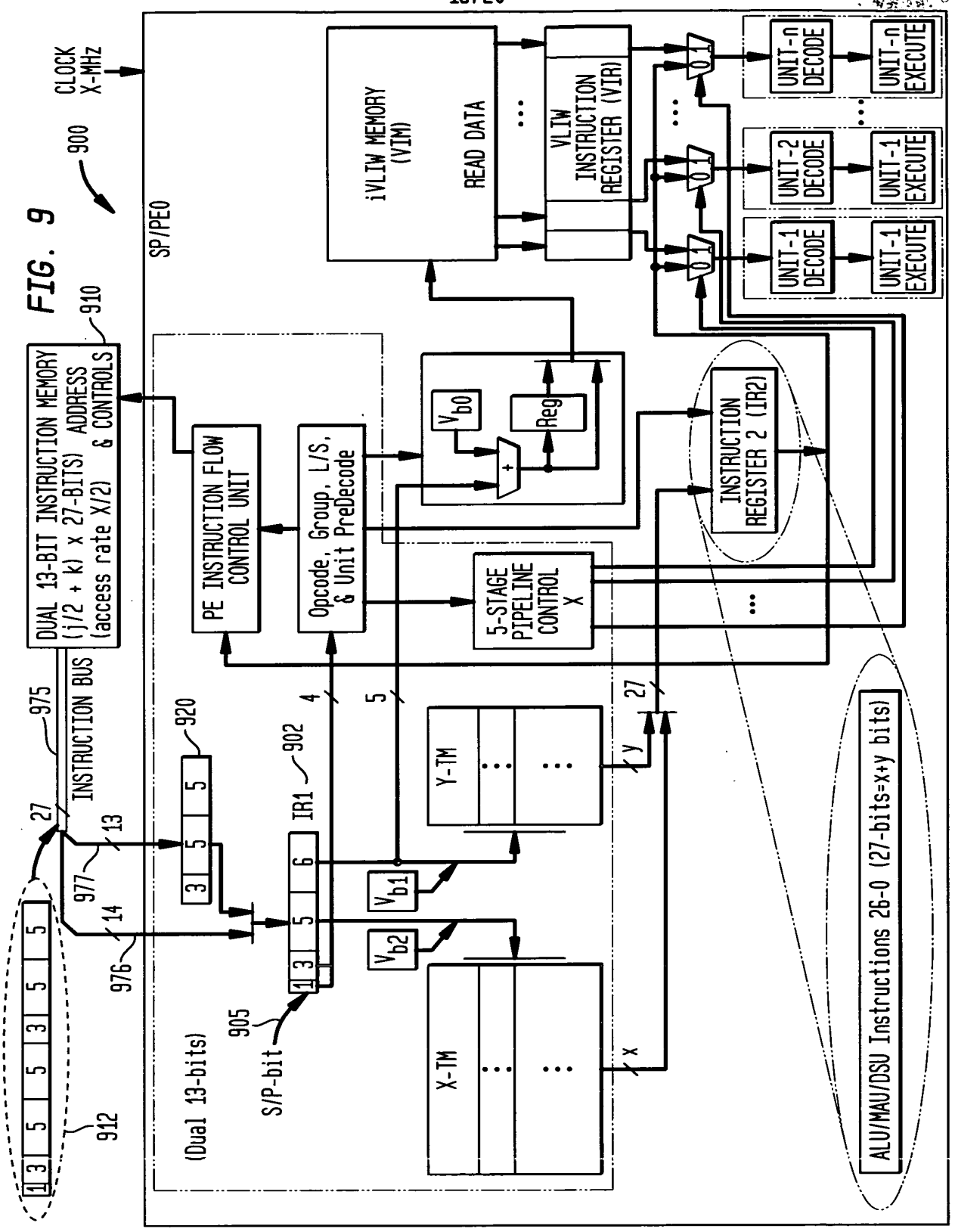
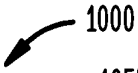

CLOCK X-MHz
900
SP/PEO
iVLIW MEMORY (VIM)
READ DATA
VLIW INSTRUCTION REGISTER (VIR)
UNIT-n DECODE
UNIT-n EXECUTE
UNIT-2 DECODE
UNIT-1 EXECUTE
UNIT-1 DECODE
UNIT-1 EXECUTE
910
DUAL 13-BIT INSTRUCTION MEMORY (i/2 + k) x 27-BITS) ADDRESS (access rate X/2) & CONTROLS
PE INSTRUCTION FLOW CONTROL UNIT
Opcode, Group, L/S, & Unit PreDecode
Vb0
Reg
INSTRUCTION REGISTER 2 (IR2)
5-STAGE PIPELINE CONTROL X
975
INSTRUCTION BUS
920
902
IR1
4
5
27
Y-TM
y
13
977
14
976
Vb1
Vb2
905
S/P-bit
(Dual 13-bits)
X-TM
x
912
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

FIG. 9

FIG. 10



1015 CYCLE	1025 FETCH	1035 Xpand & Dispatch	1045 Decode	1055 Execute	1065 Cond. Ret
1010 i	SP Fetches a B-bit Instr(i)=ADD.S instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
1020 i+1	SP Fetches a B-bit Instr(i+1)=XV.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the S/P.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
1030 i+2	SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the S/P. The VIM address is calculated and the iVLIW is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
1040 i+3	SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S instruction is loaded into IR2	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW decode	The ALU executes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)
1050 i+4	SP Fetches a B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S instruction is loaded into IR2	The DSU decodes the Instr(i+2)=COPY.S instruction	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW execute	Instr(i+1)=ADD.S side effects are set in ASFs and ACFs